A reduced power shift register with clock gating

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1. Introduction:

In [digital circuits](http://en.wikipedia.org/wiki/Digital_circuit), a shift register is a cascade of [flip flops](http://en.wikipedia.org/wiki/Flip-flop_%28electronics%29), sharing the same [clock](http://en.wikipedia.org/wiki/Clock_signal), in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "[bit array](http://en.wikipedia.org/wiki/Bit_array)" stored in it, *shifting in* the data present at its input and *shifting out* the last bit in the array, at each transition of the clock input.

More generally, a shift register may be multidimensional, such that its "data in" and stage outputs are themselves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel.

Shift registers can have both [parallel](http://en.wikipedia.org/wiki/Parallel_communication) and [serial](http://en.wikipedia.org/wiki/Serial_communication) inputs and outputs. These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in, serial-out' (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also 'bidirectional' shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected to create a 'circular shift register'.

Clock gating is a widely used technique for dynamic power reduction in VLSI design. In its most straightforward application it allows disabling the clock signal of a flip-flop once its state is no longer subject to changes. This paper extends this technique one step further and proposes a systematic way to achieve additional dynamic power savings based on the correlation of flip-flops' activities. Circuits based on shift registers are widely used in digital systems and we selected them to demonstrate the effectiveness of the proposed method. The best, worst and average cases for dynamic power savings tare analyzed.

2. Types of LFSR:

(a). Fibonacci LFSR:



Figure 1. Fibonacci LFSR

The feedback tap numbers In a 16-bit Fibonacci LFSR shown below correspond to a original polynomial thus through the maximum number of 65535 states the register cycles exclude the all-zeros state. Taps is an important concept here as the bit positions which have an influence on the subsequent state. In the diagram, for example, the taps are [16, 14, 13, 11].



Figure 2. 16-bit Fibonacci LFSR

(b). Galois LFSR:

Figure 3. Galois LFSRs

Modular refers to an LFSR in Galois with its configuration, and including internal XORs, one-to-many LFSR as well, is an alternate construction that can give rise to the same output data as a traditional LFSR. The register numbers shown below illustrate the same original polynomial as the Fibonacci example. However, they are counted in reverse to the shifting direction.



Figure 4. 16-bit Galois LFSRs

3. Fundamental components:

(a). Normal LFSR:

We call it a linear feedback shift register because it is a shift register whose input bit is a linear function of its preceding state. XOR and inverse-XOR are the only linear functions of single bits. The taps of a linear feedback shift register can be stood for as a polynomial mod.



Figure 5. Traditional LFSR

(b). Clock gating LFSR:

Linear feedback shift register with clock gating is often used to decrease power dissipation in a digital system dynamic power management. DPM strategy is taken advantage of, at circuit level, to disables the clock of FFs while the value of output is same as that of input, making the FF active only when there are distinctions between the input signal and output signal.



Figure 6. Gate-clock n-bit LFSR

4. Simulation of circuit:

Figure 7. 16 bit linear feedback shift register with clock gating

Basically, I use the same clock cycles and input vector to calculate the 16-bit linear feedback shift register with and without clock gating. I make the program using the VHDL code to fetch the picture of circuit, and finally I obtain the power from ELDO.

5. Result and comparison:

|  |  |  |
| --- | --- | --- |
|  | without clock gating(mw) | with clock gating(mw) |
| Maximum power | 38.126 | 30.375 |
| Average power | 6.014 | 5.241 |
| Minimum power | 45.986nw | 62.039nw |

Table 1. Comparison between 16 bit traditional LFSR and 16 bit clock gate LFSR

6. Conclusion:

Average power dissipation and maximum power dissipation have declined, while Minimum power has ascended which may be ascribed to the initial power consumption during the period of initializing the LFSR.

7. References:

(a). Yasmeen Khan, “power optimization of linear feedback shift register using clock gating”.

(b). Dr. Vishwani Agrawal: Slides Spring 2009.Low Power Design of Electronic Circuits.

(c). Shilesh Malliyoor, Chao You, “comparison of hardware implementation and power consumption of low-power multiple output linear feedback shift register”.